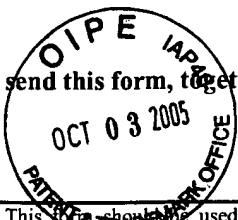


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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,884	09/22/2003	Keiji Hayashida	Q77404	4264

TITLE OF INVENTION: PHASE-LOCKED LOOP CIRCUIT REDUCING STEADY STATE PHASE ERROR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$1700	10/14/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
KINKEAD, ARNOLD M	2817	331-100000

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NEC Electronics Corporation

Kanagawa, Japan

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Date October 3, 2005

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